CLAIMS

[1] A solid state imaging device has

a plurality of unit pixels formed in an imaging area, wherein

each unit pixel has

a photoelectric converter for generating a charge in accordance with an amount of incident light,

a transfer transistor for transferring a signal of the photoelectric converter to a floating node,

an amplifier transistor for outputting a signal of the floating node to a signal line, and

a reset transistor for resetting the floating node,

at least one of a plurality of potentials supplied to a gate electrode of the reset transistor being a negative potential.

[2] A solid state imaging device with a unit pixel having:

a photoelectric converter for generating a charge in accordance with an amount of incident light,

a transfer transistor for transferring a signal of the photoelectric converter to a floating node,

an amplifier transistor for outputting a signal of the floating node to a signal line,

a reset transistor for resetting the floating node, and

a portion able to supply three or more types of

potentials to the gate electrode of the reset transistor.

[3] A solid state imaging device as set forth in claim 2, wherein the voltage of at least one type of potential among at least three or more types of potentials supplied to the gate electrode of the reset transistor is a negative potential.

[4] A solid state imaging device as set forth in claim 3, wherein the device has a portion able to set the gate potential when bringing the reset transistor from an ON state to an OFF state at a negative power source potential after passing a ground level power source potential from a positive high level power source potential.

[5] A solid state imaging device as set forth in claim 3, wherein at both timings of sampling and holding a precharge phase and a data phase, the gate potential of the reset transistor is set at the ground potential.

[6] A solid state imaging device as set forth in claim 5, wherein in a period during which the gate potential of the reset transistor of the selected pixel is set at the ground potential, the gate potential of the reset transistor of the nonselected pixel is a negative potential.

[7] A solid state imaging device as set forth in claim 1, wherein the device has a chip for processing the signal output through the signal line.

[8] A camera system having:

a solid state imaging device with a unit pixel having a photoelectric converter for generating a charge in accordance with an amount of incident light, a transfer transistor for transferring a signal of the photoelectric converter to a floating node, an amplifier transistor for outputting a signal of the floating node to a signal line, and a reset transistor for resetting the floating node, at least one of a plurality of potentials supplied to a gate electrode of the reset transistor being a negative potential;

an optical system for guiding incident light to an imaging portion of the solid state imaging device; and

a signal processing circuit for processing an output signal of the solid state imaging device.

[9] A camera system having:

a solid state imaging device with a unit pixel having a photoelectric converter for generating a charge in accordance with an amount of incident light, a transfer transistor for transferring a signal of the photoelectric converter to a floating node, an amplifier transistor for outputting a signal of the floating node to a signal line, a reset transistor for resetting the floating node, and a portion able to supply three or more types of potentials to the gate electrode of the reset transistor;

an optical system for guiding an incident light to an

imaging portion of the solid state imaging device; and

a signal processing circuit for processing an output signal of the solid state imaging device.